# Experiment no 5

# AIM: - To implement CMOS Inverter, NAND, NOR and Half Adder.

# OBJECTIVE: - To study the logic behavior of CMOS inverter, NAND, NOR and Half Adder.

**SOFTWARE:**Microwind 3.1

**THEORY: -**

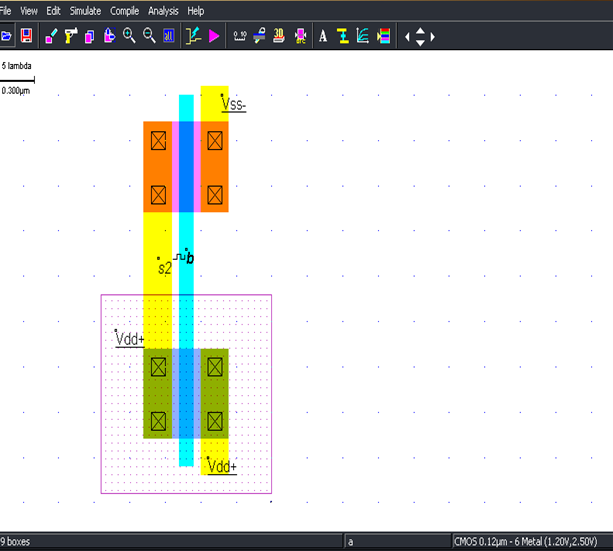
**The CMOS inverter**

The CMOS inverter design is detailed in the figure below. Here the p-channel MOS and the n-channel MOS transistors function as switches. When the input signal is logic 0 (Figure 3-4 left), the nMOS is switched off while PMOS passes VDD through the output. When the input signal is logic 1, the pMOS is switched off while the nMOS passes VSS to the output.

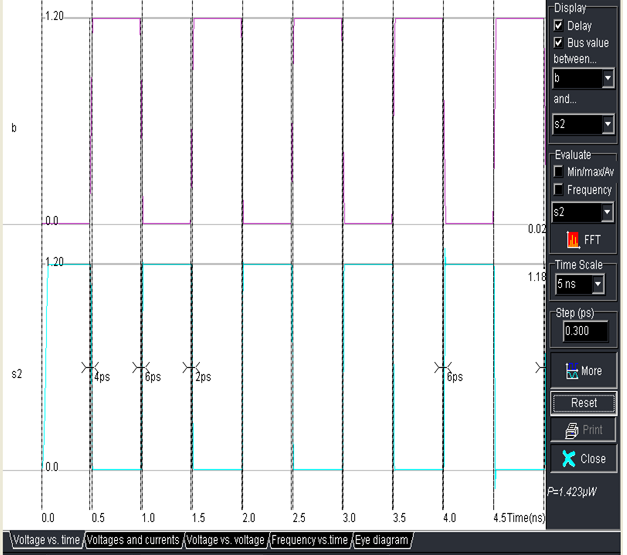


Within CMOS cells, metal and polysilicon are used as interconnects for signals. Metal is a much better conductor than polysilicon. Consequently, polysilicon is only used to interconnect gates, such as the bridge (1) between pMOS and nMOS gates, as described in the schematic diagram. Polysilicon is rarely used for long interconnects, except if a huge resistance value is expected. The procedure to create manually the layout of a CMOS inverter is described. Click the icon **MOS generator** on the palette. The following window appears. By default the proposed length is the minimum length available in the technology (2 lambda), and the width is 10 lambda. In 45-nm technology, where lambda is 20 nm (0.02 μm), the corresponding size is 0.02 μm for the length and 0.04 μm for the width. Simply click **Generate Device**, and click on the middle of the screen to fix the MOS device.Click again the icon **MOS generator** on the palette. Change the type of device by a tick on **p-channel**, andclick **Generate Device**.

Click on the top of the nMOS to fix the pMOS device. The MOS generator is the safest way to create a MOS device compliant to design rules. The programmable parameters are the MOS width, length, the number of gates in parallel and the type of device (n-channel orp-channel). By default, metal interconnects and contacts are added to the drain and source of the MOS. You may add a supplementary *metal 2* interconnect on the top of *metal 1* for drain and source.



**Waveform :**

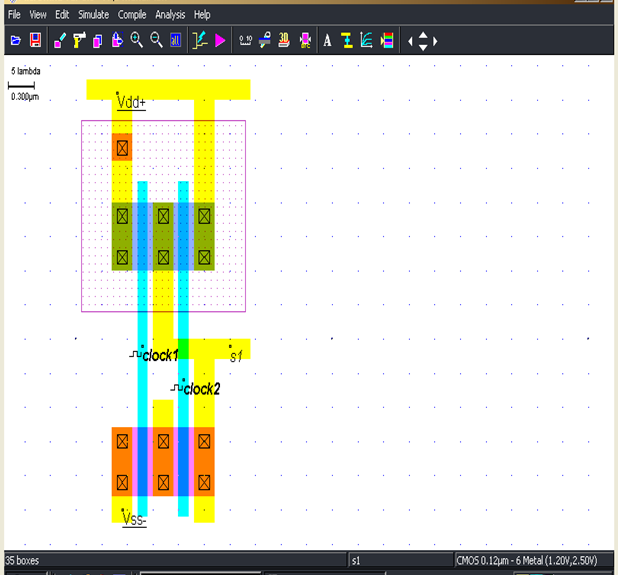


**NAND**

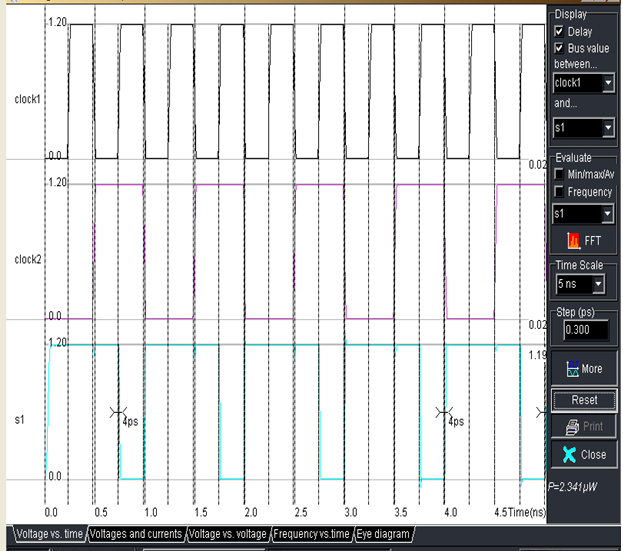
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In CMOS design, the NAND gate consists of two nMOS in series connected to two pMOS in parallel. The schematic diagram of the NAND cell is reported below. The nMOS in series tie the output to the ground for one single combination A=1, B=1.

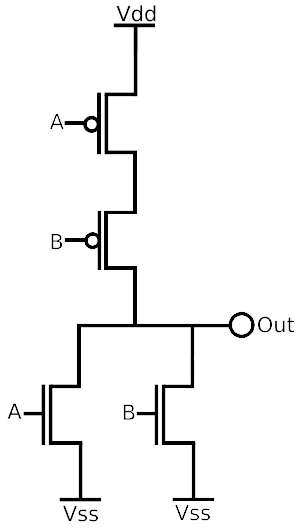
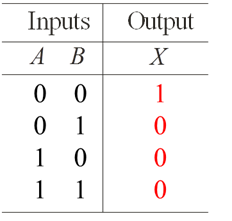


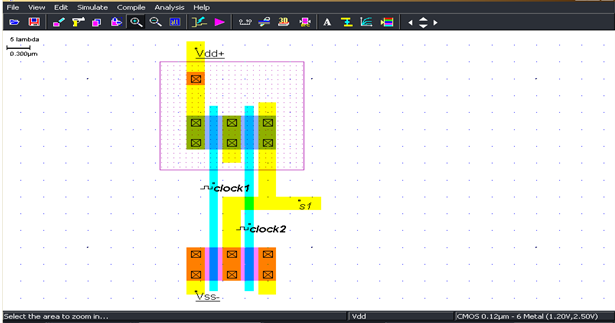
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**Waveform:**

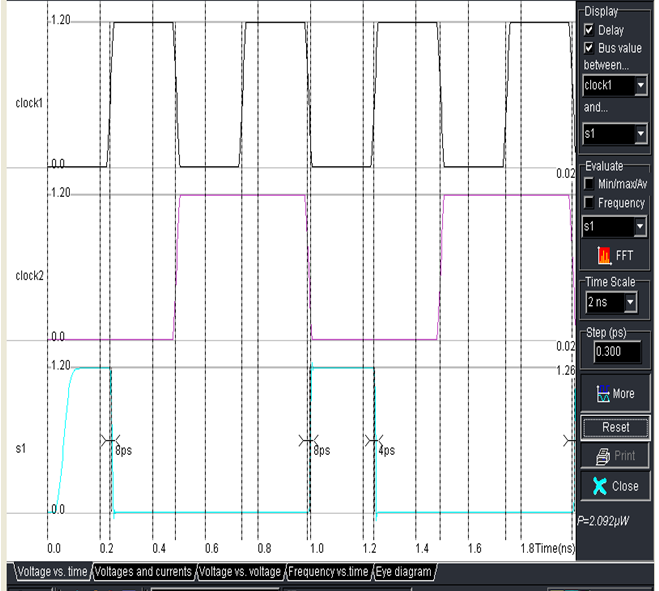
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NOR





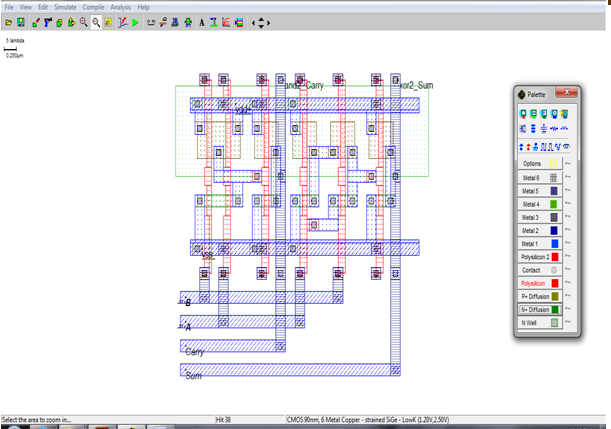
**Waveform:**



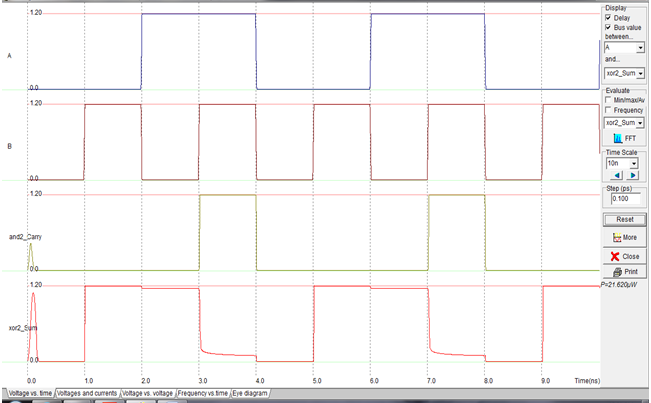
**Half Adder**

The Half-Adder gate truth-table and schematic diagram are shown in Figure. The SUM function is made with an XOR gate, the Carry function is a simple AND gate.



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Waveform:

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**Conclusion:**